The DVS Controller: Analysis and Design

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***Abstract*—High performance computing systems are undergoing exciting and rapid advancements. Increasing the portable device that operates on batteries with limited energy supply heightened the desire to reduce device power consumption based on the time varying computational workload.**

Dynamic voltage scaling (DVS) is an effective low-power design technique for reducing the dissipated power or consumption, which adjusts the supply voltage and correspondingly the clock frequency dynamically in order to obtain a minimum consumption of power to extend their lifetime use on a revolutionary scale.

This paper presents the DVS controller analysis and design for practical portable real-time applications and systems for controlling the change in the duty cycle of the DC-DC buck converter and thereby, the voltage and frequency are regulated.

Simulation and results are used to realize the controller design and verifying the range of saving power applied on realistic system workloads with varying execution times using different benchmark programs.

Keywords—Power Reduction, Voltage Scaling

I. INTRODUCTION

In high performance and digital portable design, Power dissipation has always been a crucial issue to maximize battery life, reduce cooling costs, improve reliability, and it has gained more importance and popularity in recent years [1].

Although temperature is determined by power dissipation, minimizing the power consumption of digital systems leads to a reduction in heat dissipation and cooling requirements, to reduce packaging cost of microprocessors to keep the chip at an acceptable safe bound level without unnecessarily limiting performance. It has become a first-class design constraint in microprocessor's development for high-performance computing systems including advanced architectures [2].

Dynamic supply voltage scaling (DVS) is an excellent way to reduce power consumption. The DVS unit dynamically trade processor's throughput for energy-efficiency by scaling down the supply voltage as well as clock frequency such that the actual delay of the chip meets the target performance.

The low power DVS controller design is becoming highly integrated. Several researches have been published recently in the literature of power and energy management. C. Xian et. Al. in [3] presents a DVS scheme for multitasking real-time systems with uncertain execution cycles for saving more energy than the existing solutions while guaranteeing hard deadlines. Y. Zhu and F. Mueller in [4] presents a novel approach combining feedback control with DVS schemes targeting hard real-time systems with dynamic workloads, the method relies strictly on operating system support by integrating a DVS scheduler and a feedback controller within the EDF scheduling algorithm. F. Firouzi et. al. presents an accurate formula for modelling the soft error rate of a circuit under different frequency and voltage conditions in [5], the proposed formula can be exploited in reliability-aware DVS schemes for dynamic control of energy and soft error in digital circuits. G. M. Almeida et. al. in [6] proposed a novel strategy for optimizing resources in multi-processor systems-on-Chip (MPSoC), the approach is based on using control-loop feedback mechanism, they have demonstrated the efficiency of the proposed PID controller by presenting three different scenarios. Wentong Ye et. al. presents the design of three-layer back-propagation (BP) neural network, the algorithm of BP neural network PID controller is analyzed in [7], the results showed that the PID controller based on BP neural network has good control effect in the performance of following, anti-interference, robust. S. Zhen et. al. in [8] presents an integrated high frequency and high efficiency synchronous buck converter for DVS applications, the experimental results show that high efficiency and fast reference tracking DC-DC converter brings feasible design of DVS applications.

For ensuring low power operation, and high performance DVS control unit guarantee, this work tries to analysis, design, and simulation of a digital loop for controlling the change in the duty cycle of the buck converter and thereby, the voltage and frequency are regulated, which is consistent and applicable for DVS units in allowing compact low power and fast realization of high speed and portable processors. Simulations are used to validity of theoretical background, and fundamentals have been confirmed. Results have shown that considerable amount of power consumption reduction has been confirmed and obtained.

II. THEORETICAL BACKGROUND

The algorithm of DVS technique is to maximize processor's performance while minimizing temperature and energy. Therefore, it is necessary to design a control unit which dynamically controlling microprocessor's generated temperature and dissipated power to operate whenever the processor reaches a certain temperature or average power consumed (workload), leads to reducing both of the temperature and the power dissipation. Therefore, higher performance and Power dissipation reduction has been the most important considerations behind processor generation and evolution, it has been the ultimate design criteria in computer applications and system for a long time [9]. Fig.1 shows microprocessor's clock frequency over time, the microprocessor's clock frequency has been increasing quickly and the power consumption has been increasing accordingly. The increasing of power consumption results in a raised ambient temperature. Thus the device performance is degraded and the circuit performance is less stable. However, these are differences between the desire to remain below a power bound and the need to remain below a temperature bound. If the processor exceeds its power bound, causes the overheating of the processor and other system components, it shortens the battery or UPS life, and complicates the cooling solutions of integrated circuits for heat removal, and increases the production cost. If the processor exceeds its temperature bound, causes the processor and other system components to fail. The failure rate of a processor are doubles every 10°C increase.

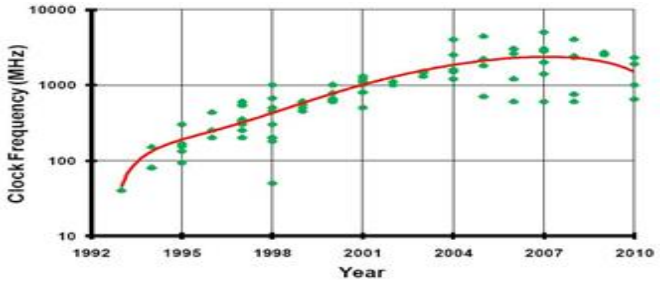

Fig. 1. Microprocessor clock frequency over time

Dynamic voltage scaling technique offer improved performance by reducing the supply voltage as the clock frequency is reduced. For a time varying or dynamic workload, the DVS allows hardware to alter dynamically the voltage-frequency of the processor (fαV). The main component of the power consumption is the dynamic power, which is proportional to (V^2f), and energy per cycle is power divided by frequency, energy consumption is proportional to frequency squared ($E\alpha f^2$), So, the processor for light workloads can run at half speed and use (1/4) of the energy to run for the same number of cycles [10].

A variable power supply can be generated using a DC-DC buck converter which takes a fixed supply voltage and can generate a variable voltage output based on a pulse-width modulated signal (PWM) by modulating the duration of the ON/OFF pulses. The PID controller is required to improve voltage scaling algorithms so that their performance remains the same but their energy consumption goes down, The schematic of simplified DVS unit is shown in Fig.2

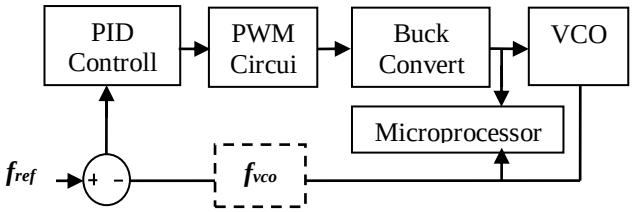

Fig. 2. Schematics of the simplified DVS unit

The generated frequency from voltage controlled oscillator (f_{vco}) is determined by the control voltage that generated from the buck converter by keeping the difference between the reference voltage (f_{ref}) and f_{vco} equal to 0. The PID controller adjusts the supply voltage V_{dd} as the difference between f_{ref} and f_{vco}, its transfer function is given by the following equation:

$$C(S) = K_p + \frac{K_i}{S} + K_d S = \frac{K_d S^2 + K_p S + K_i}{S} \qquad (1)$$

Where, K_p is proportional gain, K_i is integral gain, and K_d is derivative gain.

The purpose of PWM is to provide a variable DC voltage by translating the PID output in term of duty variable cycle pulses (D) that is then converted to the voltage V_{dd} by the buck DC-DC converter. To regulate the battery or DC voltage into a dynamically variable voltage, high performance and power efficient PID controller is required to achieve variable frequency operation to give an improvement in efficient operating range of the DVS unit, where, conventional fixed-frequency DC-DC converters cannot meet these requirements [11].

When processor's workloads vary and when the processor has less work, it can be slowed down without affecting performance adversely. Fig.3 shows the normalized energy consumption per operation versus normalized frequency.

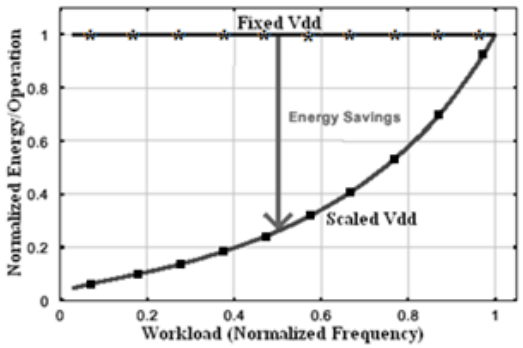

Fig. 3. Normalized energy vs. normalized frequency

The voltage is set automatically by monitoring the supply voltage and clock frequency, and then adjusting the clock frequency adaptively. The power consumption reduces dramatically for lower frequencies; its approximation on a CMOS circuit node gives the following formula:

$$P_{CMOS} = P_{dynamic} \approx \alpha f C V_{dd}^{2} \quad (2)$$

Where, α is the switching activity, and C is the load capacitance [12].

The power dissipation of digital devices is frequently subjecting to voltage breakdown and regulation; this condition is generally accompanied by an excessive change in clock frequency.

III. The Controller Design

The PID controller is a feedback controller to provide the error signal and calculates the output based on the characteristics of the signal to provide excellent control performance. It is widely used in the electronic circuits because of the ample use of proportional integral derivative controllers to maintain the stability of the control system due to its flexibility and reliability. The structure of the PID controller makes it easy to regulate the process output [6, 12].The proportional term drives a change to the output that is proportional to the current error. The integral term is proportional to both the magnitude and the duration of the error. It (when added to the proportional term) accelerates the movement of the process towards the set point and often eliminates the steady-state error that may occur with a proportional only controller [13, 14].

It is necessary to design a PID controller for adjusting the appropriated voltage/frequency of the processors at the same time, the deadline miss ratio is reduced for saving power and meeting the deadline right on time. The DVS unit will calculate an error value from the difference between the desired and obtained throughput. As output of the PID controller frequency values is indicated and send to the PWM circuit to generate variable duty cycle pulses, which will be responsible for scaling UP/DOWN the supply voltage through the use of DC-DC buck converter topology. The converter requires re-regulation of V_{dd} for a significant period of time.

The VCO output frequency is approximately has a linear proportion with the input voltage from the buck converter. Therefore, changing the applied voltage to the VCO results the variable frequency output. The procedure will be repeat until the obtained processor's throughput gradually gets closer to the desired throughput [15,16]. The block diagram of the controller and digital loop is shown in Fig.4.

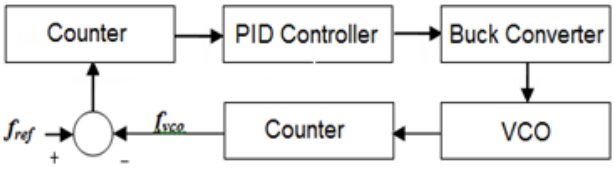

Fig. 4. The Block diagram of the DVS control loop

The operation of the digital control loop is depending on the frequency difference based on the workload predictor, these differences feeding into counters to count error differences applying to the PID controller to make possible corrections to the output and converted to voltage levels via DC-DC buck converter circuit. Therefore, the regulated required voltage will operate at the desired reference clock frequency.

The DVS digital control loop has been designed completely to varying the operating supply voltages in conjunction with clock frequency to prevent timing violations, and then, the overall loop has been simulated for different relative operating clock frequency and corresponding relative supply voltages. Simulation results have confirmed that, the control loop can reduce the significant amount of power dissipation and a significant amount of power saving has been obtained.

IV. Simulation and Results

For controlling the power dissipation and generated temperatures, the DVS control unit tries to regulate both of the supply voltage and clock frequency to maintain the processor's power until the temperature returns to a safe zone. Therefore, the simulation results are obtained in a continual range of speeds. The desired clock frequency can be obtained by running different parts of a given task at different real clock frequencies.

Different simulations are made of the DVS control loop on a machine of "3.8GHz, 3.2V, 2GB SDRAM INTEL Pentium IV processor", using different benchmark programs. Table 1 shows the simulation results of the designed DVS controller, while Fig.5 shows The line plot of simulation results (V_{dd}-f_{clk}

TABLE I. Simulation Results of the DVS Controller

V_{dd} (V)	f_{clk} (GHz)	V_{dd} (V)	f_{clk} (GHz)
3.641	3.191	2.742	2.311
3.591	3.184	2.621	2.251
3.594	3.179	2.598	2.193
3.587	3.17	2.481	2.162
3.55	3.168	2.374	1.988
3.431	2.822	2.236	1.884
3.321	2.734	2.035	1.724
3.178	2.675	2.041	1.718
3.079	2.542	1.856	1.551
3.641	3.191	2.742	2.311

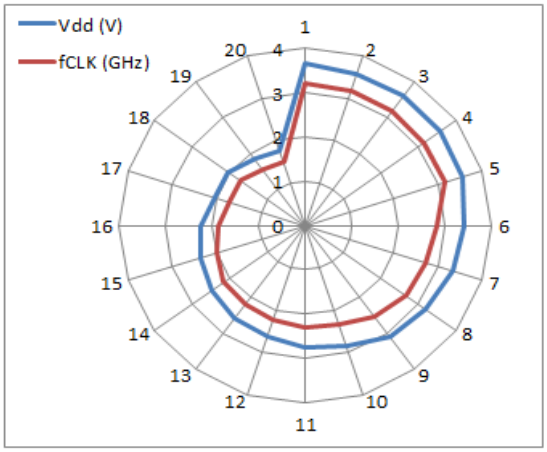

Fig. 5. The line plot of simulation results

From the resultant figure, it is obvious that, the DVS control loop for supply voltage scaling can provide significant and quadratic reduction on the dynamic power consumption on realistic workloads while meeting a time constraint. In the closed DVS loop system, the voltage is set automatically by monitoring the system's performance margin and adjusting the supply voltage adaptively that offers improved power and energy savings.

V. CONCLUSION

The Power consumption and heat dissipation become key elements in the field of high-end integrated circuits, especially those used in high speed/performance applications, due to their increase of transistor count and clock frequencies. The power dissipation reduction has become an important challenge of modern computing and portable computers. The DVS for scaling a supply voltage has received a lot of attention as an effective power management technique for digital portable systems.

In this paper a digital control loop has been analyzed, presented and simulated for voltage scaling applicable for real-time portable systems assuming that the processor can vary its supply voltage dynamically, but can use only a single voltage level at a time. The results exploit the fact that, power consumption tends to drop quadratically with voltage, while the clock frequency increasing linearly satisfying the time constraint. The controller is simple to implement and allows fast transient response to step changes in speed, and stable operation over a wide range of system clock frequencies. The simulation results confirm that, the impact of DVS technique can be considered as an excellent candidate for low power and low cost designs and cannot be overlooked because of the extraordinary growth in portable devices and systems.

Finally, for the future evolutions of this work, the presented design methodology can be improved and further analysis can be carried on, future work in this area will focus toward a new design topology for reducing power dissipation in conjunction with thermal solutions in high performance large scale multicore/multiprocessor computers.

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